

58 and 60 are reproduced below without change in order that all of the claims being prosecuted may be easily viewed together.

44. (Fourfold Amended) A pair of adjacent stacked capacitors fabricated using a photolithographic process having a characteristic minimum photolithographic feature dimension on [relative to] a semiconductor substrate, the adjacent stacked capacitors respectively including a lower plate having a minimum lateral spacing from one another which is less than [a] the minimum photolithographic feature dimension [with which the capacitors are fabricated], each lower plate including a polysilicon plug having a diameter less than the minimum photolithographic feature dimension.

1 45. (Thrice Amended) [The capacitors of claim 44] A pair of
2 adjacent stacked capacitors fabricated using a photolithographic process
3 having a characteristic minimum photolithographic feature dimension on
4 a semiconductor substrate, the adjacent stacked capacitors respectively
5 including a lower plate having a minimum lateral spacing from one
6 another which is less than the minimum photolithographic feature
7 dimension wherein each of the pair of capacitors comprises:

8 a [stem] polysilicon plug having a diameter less than the minimum
9 photolithographic feature dimension; and

10 in cross-section, at least two laterally opposed fins interconnected
11 with and projecting laterally from the [stem] plug[, the stem having a
12 minimum width which is less than the minimum photolithographic feature
13 dimension].

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15 51. The capacitors of claim 44, wherein the lower plates are
16 formed from conductive polysilicon.

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18 52. (Amended) The capacitors of claim 45, wherein the [stem]
19 plug and fins are formed from conductive polysilicon.

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21 53. The capacitors of claim 45, wherein the pair of stacked
22 capacitors are coated with a capacitor dielectric layer.
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1 54. (Amended) A pair of adjacent stacked capacitors fabricated
2 using a photolithographic process having a characteristic minimum
3 photolithographic feature dimension on [relative to] a semiconductor
4 substrate, the adjacent stacked capacitors respectively including a lower
5 plate having a minimum lateral spacing from one another which is less
6 than [a] the minimum photolithographic feature dimension, each lower
7 plate comprising a [stem] polysilicon plug having a diameter that is less
8 than the minimum photolithographic feature dimension and, in cross-
9 section, at least two laterally opposed fins interconnected with and
10 projecting laterally from the plug [stem].

11 Contd
12 E/ [Cancel claim 55.]
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14 56. (Amended) The capacitors of claim 54 wherein the [stem]
15 plug includes a minimum width which is less than the minimum
16 photolithographic feature dimension.

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18 [Cancel claim 57.]
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20 58. The capacitors of claim 54, wherein the lower plates are
21 formed from conductive polysilicon.
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1 59. (Amended) The capacitors of claim 54, wherein the [stem]
2 plug and fins are formed from conductive polysilicon.

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4 60. The capacitors of claim 54, wherein the pair of stacked
5 capacitors are coated with a capacitor dielectric layer.

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7 Cancel claim 61.

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9 62. (Amended) [The capacitors of claim 61] A pair of adjacent
10 stacked capacitors fabricated using a photolithographic process having a
11 characteristic minimum photolithographic feature dimension on a
12 semiconductor substrate, the adjacent stacked capacitors respectively
13 including a finned lower plate having a minimum lateral spacing from
14 one another which is less than the minimum photolithographic feature
15 dimension wherein each finned lower plate comprises:

16 a [stem] polysilicon plug; and

17 in cross-section, at least two laterally opposed fins interconnected
18 with and projecting laterally from the [stem] plug, the [stem] plug having
19 a minimum width which is less than the minimum photolithographic
20 feature dimension.

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22 Cancel claims 63-65.

Contd
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66. (Amended) The capacitors of claim [61] 62, wherein the lower plates are formed from conductive polysilicon.

67. (Amended) The capacitors of claim 62, wherein the [stem] plug and fins are formed from conductive polysilicon.

68. (Amended) The capacitors of claim [61] 62, wherein the pair of stacked capacitors are coated with a capacitor dielectric layer.

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